PCI8305

User's Manual

Beijing ART Technology Development Co., Ltd.

Contents

Chapter 1 Overview

In the fields of Real-time Signal Processing, Digital Image Processing and others, high-speed and high-precision data acquisition modules are demanded. ART PCI8305 data acquisition module, which brings in advantages of similar products that produced in china and other countries, is convenient for use, high cost and stable performance.

ART PCI8305 is a data acquisition module based on PCI bus. It can be directly inserted into IBM-PC/AT or a computer which is compatible with PCI8305 to constitute the laboratory, product quality testing center and systems for different areas of data acquisition, waveform analysis and processing. It may also constitute the monitoring system for industrial production process.

Software

Analysis Software

ART PCI8305 module is well-suited for precision data acquisition analysis applications, which you can specifically address with the ART Data Acquisition Measurement Suite. The suite has two components –digital and graphics mode analysis (functions) for voltage (any signal can be transformed into the voltage signal), frequency response and other analysis.

Unpacking Checklist

Check the shipping carton for any damage. If the shipping carton and contents are damaged, notify the local dealer or sales for a replacement. Retain the shipping carton and packing material for inspection by the dealer.
Check for the following items in the package. If there are any missing items, contact your local dealer or sales.

- PCI8305 Data Acquisition Board
- ART Disk
  1) user's manual (pdf)
  2) drive
  3) catalog
- Warranty Card

FEATURES

Analog Input

- Input Range: ±10V, ±5V, ±2.5, 0~10V
- 13-bit resolution, the 13-th bit is sign bit
- Sampling Rate: 180KS/s
- Input Channels: 16SE/8DI
- Isolated voltage; 2500Vrms (1 min)
- Data Read Mode: software inquire, non-empty and half-full mode
- FIFO Size: 16K word
- Memory Sign: non-empty, half-full, full (overflow)
- Sample mode: continuous sample and group sample
- Group Interval: software-configurable, minimum value is sampling period, maximum value is 419430uS
- Clock Source: internal clock and external clock
- Trigger Mode: software trigger and hardware trigger (external trigger)

- Trigger Type: edge trigger and level trigger
- Trigger Dir: negative, positive, either positive or negative trigger
- Trigger Source: DTR
- DTR range: TTL
- A/D Conversion Time: ≤1.6uS
- Programmable amplifier: AD8251(default), AD8250, AD8253
- Programmable Gain: 1, 2, 4, 8 (AD8251 default) or 1, 2, 5, 10 (AD8250) or 1, 10, 100, 1000 (AD8253)
- Analog Input Impedance: 10MΩ
- Amplifier Set-up Time: 785nS(0.001%)(max)
- Non-linear error: ±3LSB(Maximum)
- System Measurement Accuracy: 0.1%
- Operating Temperature Range: 0℃~50℃
- Storage Temperature Range: −20℃~70℃

Analog Output

- Output Range: 0~5V, 0~10V, 0~10.8V, ±10V, ±10.8V
- 12-bit resolution
- Set-up Time: 10µS (0.01%)
- Output Channels: 4
- Non-linear error: ±1LSB (Max)
- Output error (full-scale): ±1LSB

Timer/Counter

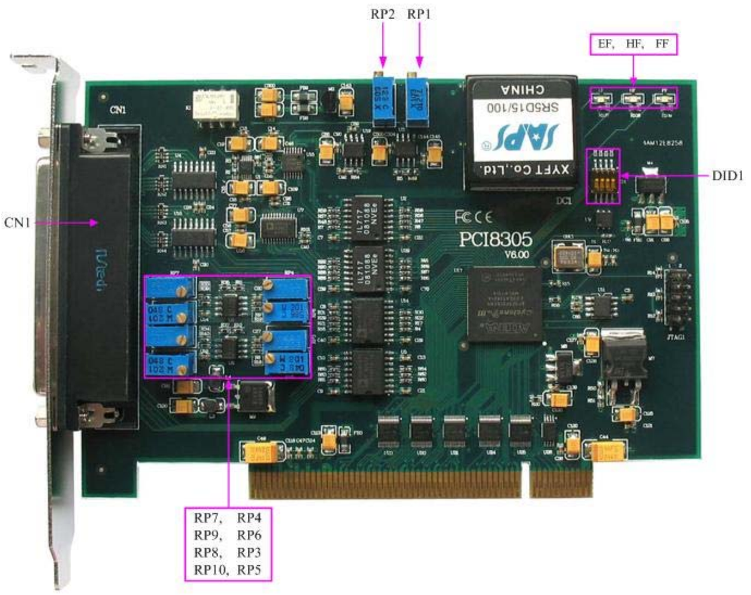
- Counter Channel No.: 3 independent counter
- Counter Mode: subtract count
- Counter Resolution: 32-bit
- Count Mode: six count modes (software-configurable)
- electrical standard: TTL compatible

Other features

- Board Clock Oscillation: 40MHz
- Board Dimensions: 144mm (L) x 98mm (W) x 17mm (H)

Chapter 2 Components Layout Diagram and a Brief Description

2.1 The Main Component Layout Diagram



2.2 The Function Description for the Main Component

2.2.1 Signal Input and Output Connectors

CN1: Signal input and output connectors

2.2.2 Potentiometer

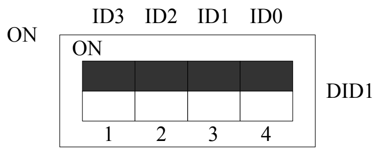
RP1: Analog input zero point adjustment potentiometer
RP2: Analog input full-scale adjustment potentiometer
RP4, RP7, RP3, RP8: AO0~AO3 zero point adjustment potentiometer
RP6, RP9, RP5, RP10: AO0~AO3 full-scale adjustment potentiometer

2.2.3 Status Indicator

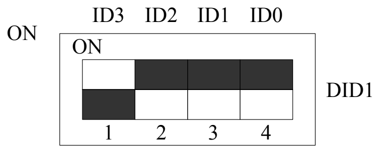
EF: FIFO non-empty status indicator
HF: FIFO half-full status indicator
FF: FIFO overflow status indicator

2.2.4 Physical ID of DIP Switch

DID1: Set physical ID number. When the PC is installed more than one PCI8305 , you can use the DIP switch to set a physical ID number for each board, which makes it very convenient for users to distinguish and visit each board in the progress of the hardware configuration and software programming. The following 4-bit numbers are expressed by the binary system: When DIP switch points to "ON", that means "1", and when it points to the other side, that means "0." As they are shown in the following diagrams: "ID3" is the high bit. "ID0" is the low bit, and the black part in the diagram represents the location of the switch. (Test softwares of the company often use the logic ID management equipments and at this moment the physical ID DIP switch is invalid. If you want to use more than one kind of the equipments in one and the same system at the same time, please use the physical ID as much as possible.).



The above chart shows"1111", so it means that the physical ID is 15.



The above chart shows"0111", so it means that the physical ID is 7.

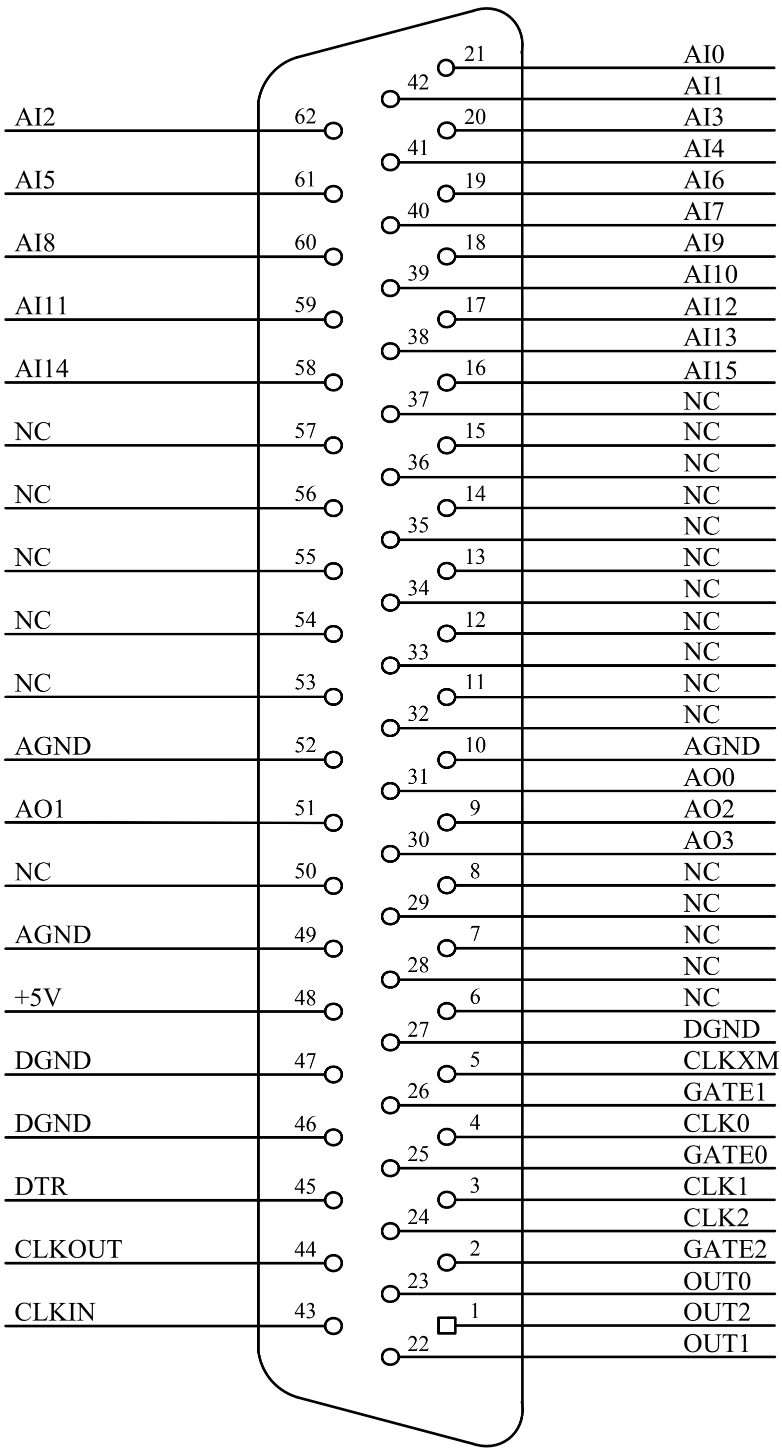
The above chart shows"0101", so it means that the physical ID is 5.

ID3	ID2	ID1	ID0	Physical ID（Hex）	Physical ID（Dec）
OFF（0）	OFF（0）	OFF（0）	OFF（0）	0	0
OFF（0）	OFF（0）	OFF（0）	ON（1）	1	1
OFF（0）	OFF（0）	ON（1）	OFF（0）	2	2
OFF（0）	OFF（0）	ON（1）	ON（1）	3	3
OFF（0）	ON（1）	OFF（0）	OFF（0）	4	4
OFF（0）	ON（1）	OFF（0）	ON（1）	5	5
OFF（0）	ON（1）	ON（1）	OFF（0）	6	6
OFF（0）	ON（1）	ON（1）	ON（1）	7	7
ON（1）	OFF（0）	OFF（0）	OFF（0）	8	8
ON（1）	OFF（0）	OFF（0）	ON（1）	9	9
ON（1）	OFF（0）	ON（1）	OFF（0）	A	10
ON（1）	OFF（0）	ON（1）	ON（1）	B	11
ON（1）	ON（1）	OFF（0）	OFF（0）	C	12
ON（1）	ON（1）	OFF（0）	ON（1）	D	13
ON（1）	ON（1）	ON（1）	OFF（0）	E	14
ON（1）	ON（1）	ON（1）	ON（1）	F	15

Chapter 3 Signal Connectors

3.1 The Definition of Signal Input and Output Connectors

62 core plug on the CN1 pin definition



Pin definition about CN1:

Pin name	Pin feature	Pin function definition
AI0~AI15	Input	Analog input, reference ground is AGND.
AO0~AO3	Output	Analog output, reference ground is AGND.
AGND	GND	Analog ground. This AGND pin should be connected to the system's AGND plane.
DGND	GND	Digital ground. This DGND pin should be connected to the system's DGND plane.
CLKIN	Input	External clock input.
CLKOUT	Output	Internal clock output.
DTR	Input	Digital trigger input.
CLKXM	Output	On-board clock oscillator pulse output, can provide clock source signal for CLK0~CLK2.
CLK0～CLK2	Input	Counter 0~3 clock input
GATE0~GATE2	Input	Counter 0~3gate.
OUT0~OUT2	Output	Counter 0~3output.
+5V	Output	5V power supply output.
NC	--	Not connected.

Chapter 4 Connection Ways for Each Signal

4.1 Analog signal single-ended input connection

Single-ended mode can achieve a signal input by one channel, and several signals use the common reference ground. This mode is widely applied in occasions of the small interference and relatively many channels.

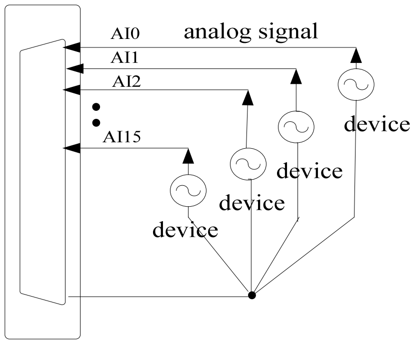


Figure 4.1 single-ended input connection

4.2 Analog differential inputs

Double-ended input mode, which was also called differential input mode, uses positive and negative channels to input a signal. This mode is mostly used when biggish interference happens and the channel numbers are few. SE/DI mode can be set by the software, please refer to PCI8305 software manual.

According to the diagram below, PCI8305 board can be connected as analog voltage double-ended input mode, which can effectively suppress common-mode interference signal to improve the accuracy of acquisition. Positive side of the 8-channel analog input signal is connected to AI0~AI7, the negative side of the analog input signal is connected to AI8~AI15, equipments in industrial sites share the AGND with PCI8305 board.

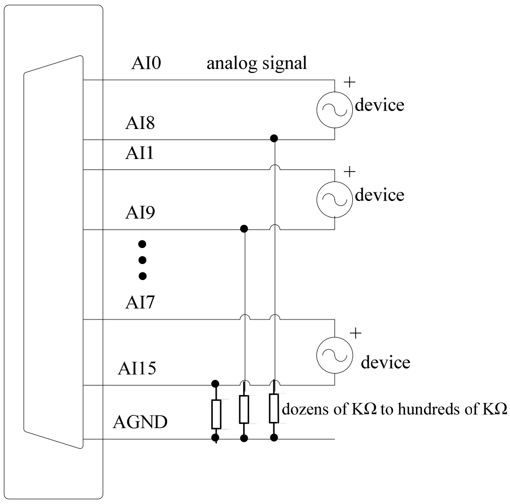


Figure 4.2 double-ended input connection

4.3 Analog output connection

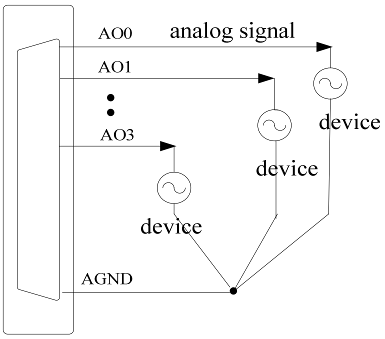
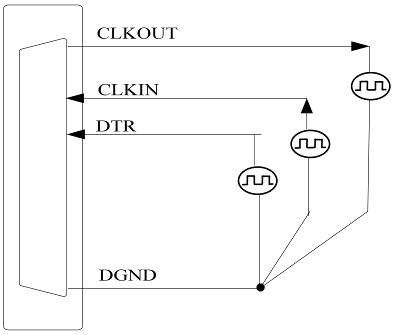
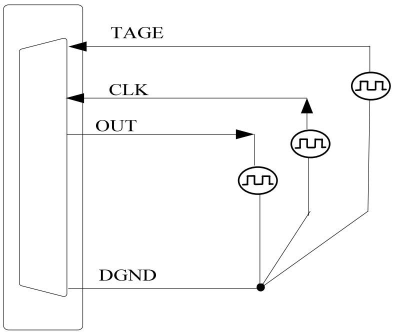


Figure 4.3 analog signal output connection

4.4 Clock input/output and trigger input connection



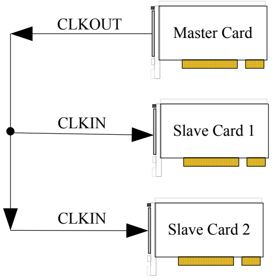
4.5 Timer/counter connection



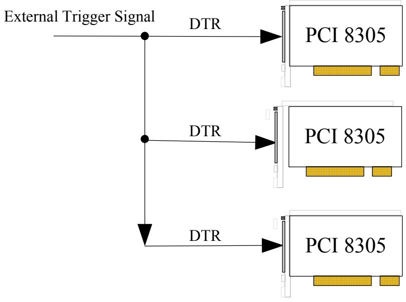
4.6 Methods of Realizing the Multi-card Synchronization

Three methods can realize the synchronization for the PC8305, the first method is using the cascade master-slave card, the second one is using the common external trigger, and the last one is using the common external clock.

When using master-slave cascade card programs, the master card generally uses the internal clock source model, while the slave card uses the external clock source mode. After the master card and the slave card are initialized according to the corresponding clock source mode. At first, start all the slave cards, as the main card has not been activated and there is no output clock signal, so the slave card enters the wait state until the main card was activated. At this moment, the multi-card synchronization has been realized. When you need to sample more than channels of a card, you could consider using the multi-card cascaded model to expand the number of channels.

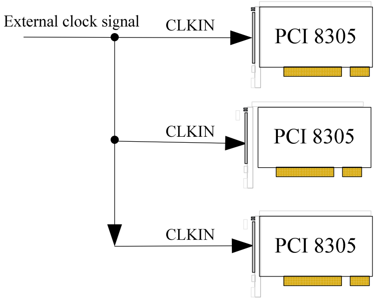


When using the common external trigger, please make sure all parameters of different PCI8305 are the same. At first, configure hardware parameters, and use digital signal triggering (DTR), then connect the sampled signal, input triggering signal from DTR pin, then click “Start” button, at this time, PCI8305 does not sample any signal but waits for external trigger signal. When each module is waiting for external trigger signal, use the common external trigger signal to startup modules, at last, we can realize synchronization data acquisition in this way. See the following figure:



Note: when using the DTR, select the internal clock mode

When using the common external clock trigger, please make sure all parameters of different PCI8305 are the same. At first, configure hardware parameters, and use external clock, then connect the sampled signal, then click “Start” button, at this time, PCI8305 does not sample any signal, but wait for external clock signal. When each module is waiting for external clock signal, use the common external clock signal to startup modules, at last, we realize synchronization data acquisition in this way. See the following figure:



Chapter 5 The Instruction of the A/D Trigger Function

5.1 A/D Internal Trigger Mode

When A/D is in the initialization, if the A/D hardware parameter ADPara.TriggerMode = PCI8305_TRIGMODE_SOFT, we can achieve the internal trigger acquisition. In this function, when calling the StartDeviceProAD function, it will generate A/D start pulse, A/D immediately access to the conversion process and not wait for the conditions of any other external hardware. It also can be interpreted as the software trigger.

As for the specific process, please see the figure below, the cycle of the A/D work pulse is decided by the sampling frequency.

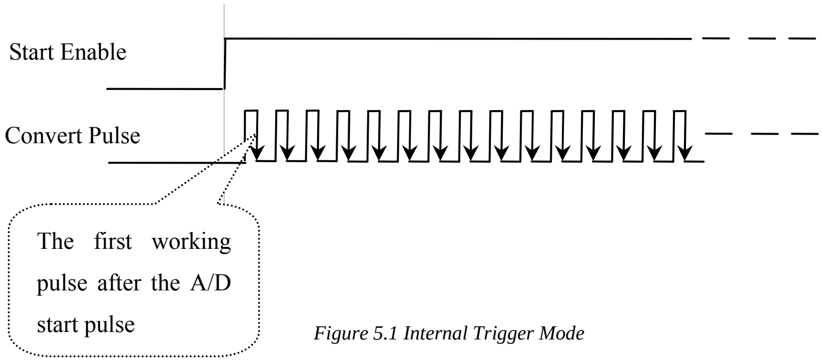


Figure 5.1 Internal Trigger Mode

5.2 A/D External Trigger Mode

When A/D is in the initialization, if the A/D hardware parameter ADPara.TriggerMode = PCI8305_TRIGMODE_POST, we can achieve the external trigger acquisition. In this function, when calling the StartDeviceProAD function, A/D will not immediately access to the conversion process but wait for the external trigger source signals accord with the condition, then start converting the data. It also can be interpreted as the hardware trigger. Trigger source is DTR (Digital Trigger Source).

(1) Edge trigger function

Edge trigger is to capture the characteristics of the changes between the trigger source signal and the trigger level signal to trigger A/D conversion.

When ADPara.TriggerDir = PCI8305_TRIGDIR_NEGATIVE, choose the trigger mode as the falling edge trigger. That is, when the DTR trigger signal is on the falling edge, A/D will immediately access to the conversion process, and its follow-up changes have no effect on A/D acquisition.

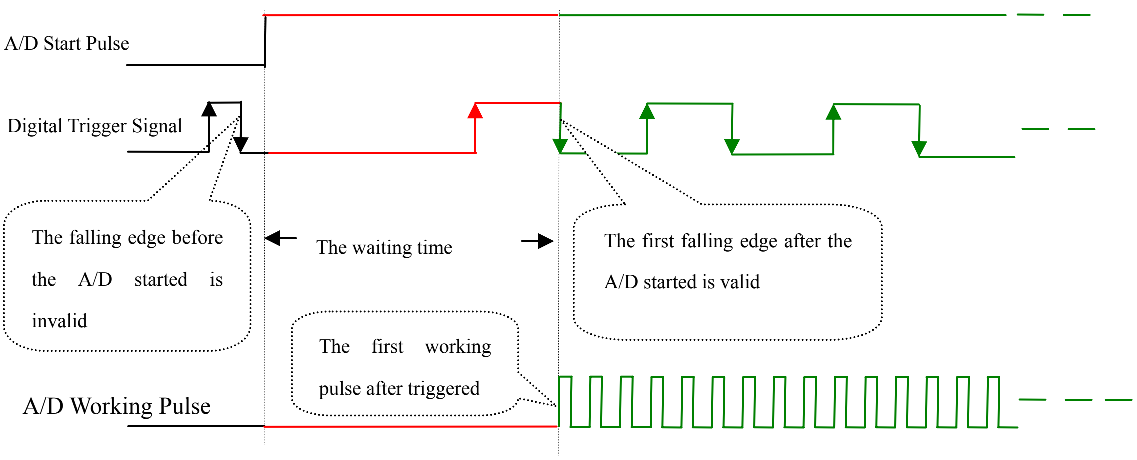


Figure 5.2.1 Falling edge Trigger

When ADPara.TriggerDir = PCI8305_TRIGDIR_POSITIVE, choose the trigger mode as rising edge trigger. That is, when the DTR trigger signal is on the rising edge, A/D will immediately access to the conversion process, and its follow-up changes have no effect on A/D acquisition.

When ADPara.TriggerDir = PCI8305_TRIGDIR_POSIT_NEGAT, choose the trigger mode as rising or falling edge trigger. That is, when the DTR trigger signal is on the rising or falling edge, A/D will immediately access to the conversion process, and its follow-up changes have no effect on A/D acquisition. This function can be used in the case that the acquisition will occur if the exoteric signal changes.

（2）Level trigger function

Level trigger is to capture the condition that trigger signal is higher or lower than the trigger level to trigger A/D conversion.

When ADPara.TriggerDir = PCI8305_TRIGDIR_NEGATIVE, it means the trigger level is low. When DTR trigger signal is in low level, A/D is in the conversion process, once the trigger signal is in the high level, A/D conversion will automatically stop, when the trigger signal is in the low level again, A/D will re-access to the conversion process, that is, only converting the data when the trigger signal is in the low level.

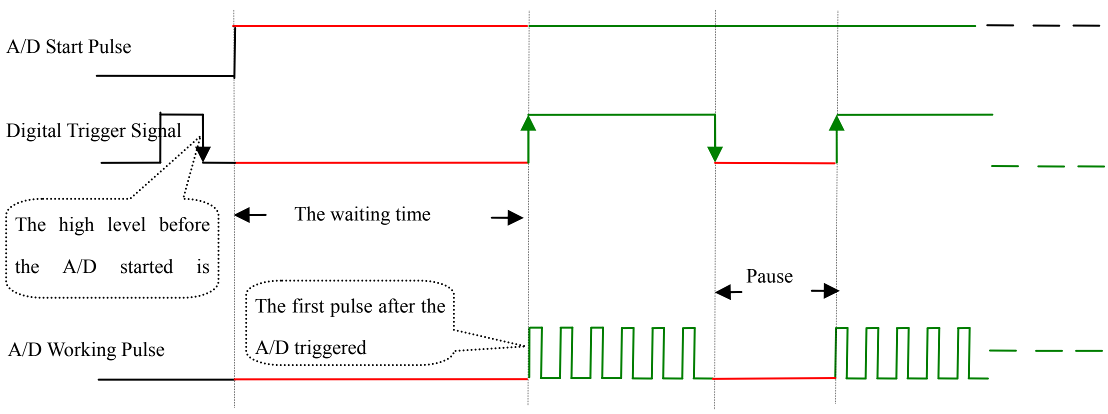


Figure 5.2.4 High Level Trigger

When ADPara.TriggerDir = PCI8305_TRIGDIR_POSITIVE, it means the trigger level is high. When DTR trigger signal is in high level, A/D is in the conversion process, once the trigger signal is in the low level, A/D conversion will automatically stop, when the trigger signal is in the high level again, A/D will re-access to the conversion process, that is, only converting the data when the trigger signal is in the high level.

When ADPara.TriggerDir = PCI8305_TRIGDIR_POSIT_NEGAT, it means the trigger level is low or high. The effect is the same as the internal software trigger.

Chapter 6 Methods of using A/D Internal and External Clock Function

6.1 Internal Clock Function of A/D

Internal Clock Function refers to the use of on-board clock oscillator and the clock signals which are produced by the user-specified frequency to trigger the A/D conversion regularly. To use the clock function, the hardware parameters ADPara.ClockSource = PCI8305 _CLOCKSRC_IN should be installed in the software. The frequency of the clock in the software depends on the hardware parameters ADPara.Frequency. For example, if Frequency = 100000, that means A/D work frequency is 100000Hz (that is, 100 KHz, 10μs / point).

6.2 External Clock Function of A/D

External Clock Function refers to the use of the outside clock signals to trigger the A/D conversion regularly. The clock signals are provide by the CLKIN pin of the CN1 connector. The outside clock can be provided by PCI8305 clock output (CLKOUT of CN1), as well as other equipments, for example clock frequency generators. To use the external clock function, the hardware parameters ADPara.ClockSource = PCI8305_CLOCKSRC_OUT should be installed in the software. The clock frequency depends on the frequency of the external clock, and the clock frequency on-board (that is, the frequency depends on the hardware parameters ADPara.Frequency) only functions in the packet acquisition mode and its sampling frequency of the A/D is fully controlled by the external clock frequency.

6.3 Methods of Using A/D Continuum and Grouping Sampling Function

6.3.1 A/D Continuum Sampling Function

The continuous acquisition function means the sampling periods for every two data points are completely equal in the sampling process of A/D, that is, completely uniform speed acquisition, without any pause, so we call that continuous acquisition.

To use the continuous acquisition function, the hardware parameters ADPara.ADMode = PCI8305 _ADMODE_SEQUENCE should be installed in the software. For example, in the internal clock mode, hardware parameters ADPara.Frequency = 100000 (100KHz) should be installed, and 10 microseconds after the A/D converts the first data point, the second data point conversion starts, and then 10 microseconds later the third data point begins to convert, and so on.

6.3.2 A/D Grouping Sampling Function

Grouping acquisition (pseudo-synchronous acquisition) function refers to the sampling clock frequency conversion among the channels of the group in the AD sampling process, and also a certain waiting time exists between every two groups, this period of time is known as the Group Interval. Loops of group refer to numbers of the cycle acquisition for each channel in the same group. In the internal clock mode and the fixed-frequency external clock mode, the time between the groups is known as group cycle. The conversion process of this acquisition mode as follows: a short time stop after the channels conversion in the group (that is, Group Interval), and then converting the next group, followed by repeated operations in order, so we call it grouping acquisition.

The purpose of the application of the grouping acquisition is that: at a relatively slow frequency, to ensure that all of the time difference between channels to become smaller in order to make the phase difference become smaller, thus to ensure the synchronization of the channels, so we also say it is the pseudo-synchronous acquisition function. In a group, the higher the sampling frequency is, the longer Group Interval is, and the better the relative synchronization signal is. The sampling frequency in a group depends on ADPara. Frequency, Loops of group depends on ADPara.LoopsOfGroup, the Group Interval depend on ADPara. Group Interval.

Based on the grouping function, it can be divided into the internal clock mode and the external clock mode. Under the internal clock mode, the group cycle is decided by the internal clock sampling period, the total number of sampling channels, Loops of group and Group Interval together. In each cycle of a group, AD only collects a set of data. Under the external clock mode, external clock cycle ⩾ internal clock sampling cycle × the total number of sampling channels × Loops of group + AD chip conversion time, AD data acquisition is controlled and triggered by external clock. The external clock mode is divided into fixed frequency external clock mode and unfixed frequency external clock mode. Under the fixed frequency external clock mode, the group cycle is the sampling period of the external clock.

The formula for calculating the external signal frequency is as follows:

Under the internal clock mode:
Group Cycle = the internal clock sampling period × the total number of sample channels × Loops of group + AD chips conversion time + Group Interval
External signal cycle = (cycle signal points / Loops of group) × Group Cycle
External signal frequency = 1 / external signal cycle

Under the external clock mode: (a fixed-frequency external clock)
Group Cycle = external clock cycle
External signal cycle = (cycle signal points / Loops of group) × Group Cycle
External signal frequency = 1 / external signal cycle

Formula Notes:
The internal sampling clock cycle = 1 / (AD Para. Frequency)
The total number of sampling channels = AD Para. Last Channel – AD Para. First Channel + 1
Loops of group == ADPara.LoopsOfGroup
AD Chips conversion time = see "AD Analog Input Function" parameter
Group Interval = AD Para. Group Interval
Signal Cycle Points = with the display of the waveform signal in test procedures, we can use the mouse to measure the signal cycle points.

Under the internal clock mode, for example, sample two-channel 0, 1, and then 0 and 1 become a group. Sampling frequency (Frequency) = 100000Hz (cycle is 10μs), Loops of group is 1, Group Interval = 50μs, then the acquisition process is to collect a set of data first, including a data of channel 0 and a data of channel 1. We need 10μs to sample the two data, 20μs to convert the data from the two channels. After the conversion time of an AD chip, AD will automatically cut-off to enter into the waiting state until the 50μs group interval ends. We start the next group, begin to convert the data of channel 0 and 1, and then enter into the waiting state again, and the conversion is going on in this way, as the diagram following shows:

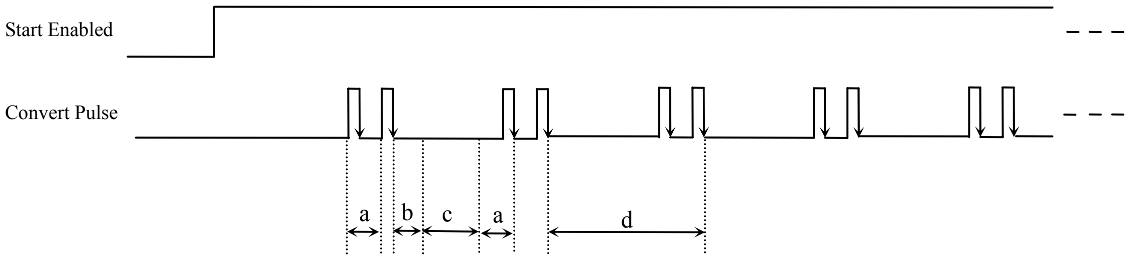


Figure 6.1 Grouping Sampling which grouping cycle No is 1 under the Internal Clock Mode

Note: a— internal clock sample cycle
b— AD chips conversion time
c—Group Interval
d— group cycle

Change the loops of group into 2, then the acquisition process is to collect the first set of data, including two data of channel 0 and two data of channel 1, the conversion order is 0,1,0,1. We need 10μs to sample each of the four data. After the conversion time of an AD chip, AD will automatically stop to enter into the waiting state until the 50μs Group Interval ends. We start the next group, begin to convert the data of channel 0 and 1, and then enter into the waiting state again, and the conversion is going on in this way, as the diagram following shows:

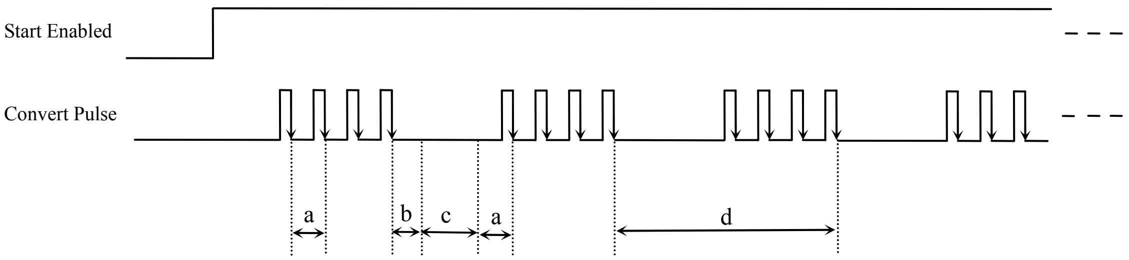


Figure 6.2 Grouping Sampling which grouping cycle No is 2 under the Internal Clock Mode

Notes: a— internal clock sample cycle
b— AD chips conversion time
c—Group Interval
d— group cycle

Under the external clock mode, the requirement is: the external clock cycle ≥ the internal clock sampling period × the total number of sampling channels× Loops of group + AD chip conversion time, otherwise, the external clock appearing in the group conversion time will be ignored.

Under the fixed-frequency external clock mode, for example, when sampling data of two-channel 0, 1, then channel 0 and channel 1 consist of a group. Sampling frequency (Frequency) = 100000Hz (the cycle is 10μs), Loops of group is 2, then the acquisition process is to collect the first set of data, including two data of channel 0 and two data of channel 1, the order of conversion 0,1,0,1, We need 10μs to sample the four data and 40μs to convert of the four data. After the conversion time of an AD chip, AD will automatically stop to enter into the waiting state until the next edge of the external clock triggers AD to do the next acquisition, and the conversion is going on in this way, as the diagram following shows:

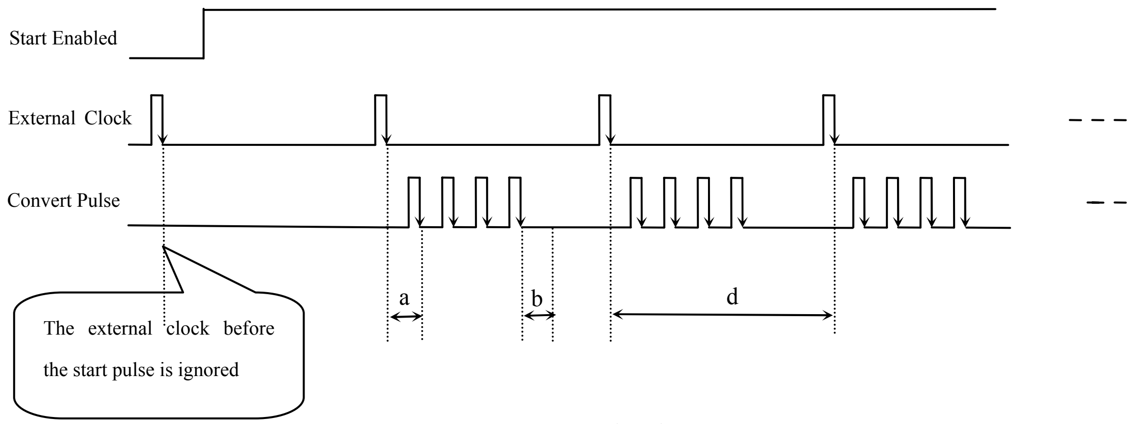


Figure 6.3 Grouping sampling under the fixed frequency external clock mode

Notes: a— internal clock sample cycle
b—AD chips conversion time
d—group cycle（external clock cycle）

Under an unfixed-frequency external clock mode, for example, the grouping sampling principle is the same as that of the fixed-frequency external clock mode. Under this mode, users can control any channel and any number of data. Users will connect the control signals with the clock input of the card (CLKIN), set the sampling channels and Loops of group. When there are external clock signals, it will sample the data which is set by users. Because the external clock frequency is not fixed, the size of external clock cycle is inconsistent but to meet: the external clock cycle ≥ the internal clock sampling period × the total number of sampling channels × Loops of group + AD chip conversion time, , otherwise, the external clock edge appearing in the group conversion time will be ignored.

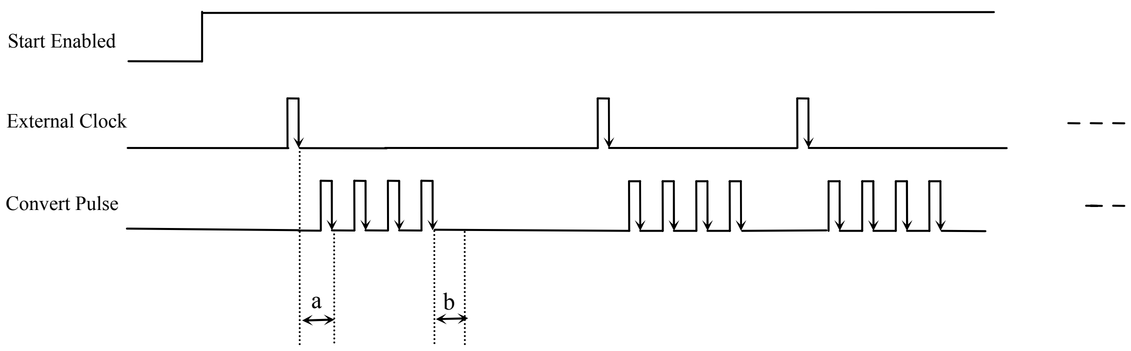


Figure 6.4 Grouping sampling under the not fixed frequency external clock mode

Note: a— internal clock sample cycle
b—AD chips conversion time

Chapter7 Subtractive Counter

Mode 0: Interrupt on terminal count

Under this mode, when given the initial value, if GATE is high level, the counter immediately begins to count by subtracting “1” each time, the counter output OUT turns into low level; when the count ends and the count value becomes 0, the counter output OUT becomes and keeps high level until given the initial value or reset. If a counter which is counting is given a new value, the counter will begin to count from the new value by subtracting “1” each time. GATE can be used to control the count, GATE=1 enables counting; GATE=0 disables counting.

OUT signal changes high from low can be used as interrupt request.

Time diagram is shown in Figure 1.

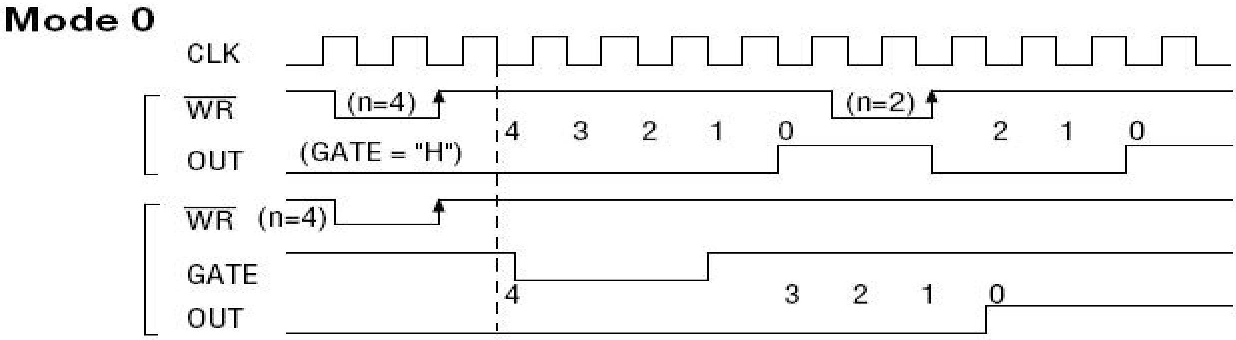


Figure 1

Mode 1: Hardware retriggerable one-shot

The mode can work under the role of GATE. After given the initial count value N, OUT becomes high level, the counter begins to count until the appearance of the rising edge of GATE, at this moment OUT turns into low level; when the count ends and the count value becomes 0, OUT becomes high level, that is, the output one-shot pulse width is determined by the initial count value N. If the current operation does not end and another rising edge of GATE appears, then the current count stops, the counter begins to count from N once again, and then the output one-shot pulse will be widened. When the count reduction of the counter has not yet reached zero, but it is given a new value N1. Only when it is the rising edge of GATE, the counter starts to count from N1.

Time diagram is shown in Figure 2.

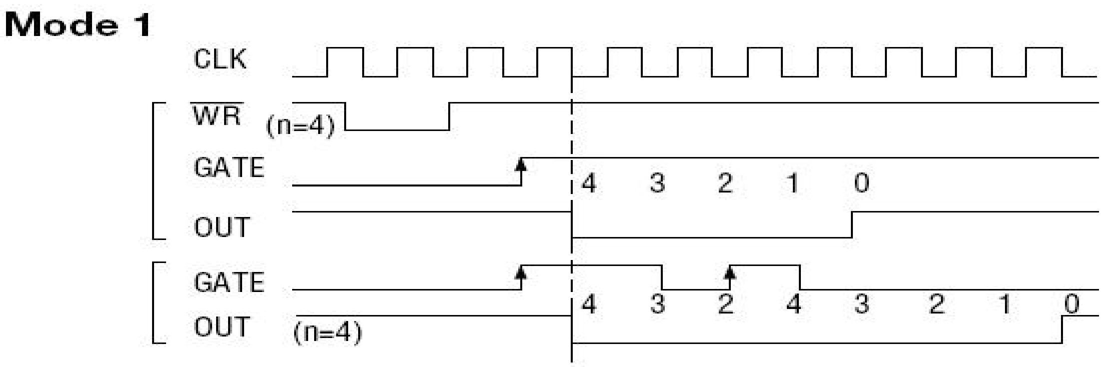


Figure 2

Mode 2: Rate Generator

Under this mode, the counter is given the initial count value N and begins to count from (N-1), OUT becomes high level. When the count value becomes 0, OUT turns into low level. After a CLK cycle, OUT resumes high level, and the counter automatically load the initial value N and begin to count from (N-1). Thus the output will continue to output a negative pulse, its width is equal to one clock cycle, the clock number between the two negative pulses is equal to the initial value that is given to the counter. GATE=1 enables counting; GATE=0 disables counting. GATE has no effect on OUT. If change the initial count when counting, it will be effective next time.
Time diagram is shown in figure 3.

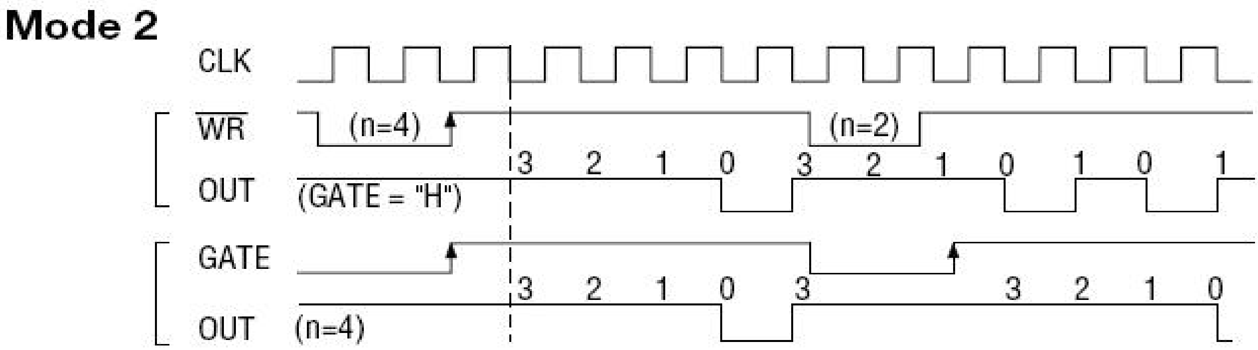


Figure 3

Mode 3: Square wave mode

Similar to Mode 2, the counter is given the initial count value N and begins to count from (N-1). When the signal of GATE is high level, it starts to count, timer/counter begins to count by subtracting “1” each time, more than half the initial count value. The output OUT has remained high level, when the count value is more than half of the initial count value; but the output OUT becomes low level, when the count value is less than half of the initial value. If the initial count value N is an even number, the output is 1:1 square-wave; if the initial count value N is an odd number, the output OUT has remained high level during the previous (n +1)/2 count period; but the output OUT becomes low level during the post (n-1)/2 count period, that is, the high level has one clock cycle more than the low level. If change the initial count when counting, it will be effective next time. When GATE = 0, the count is prohibited, when GATE = 1, the count is permitted. Time diagram is shown in figure 4.

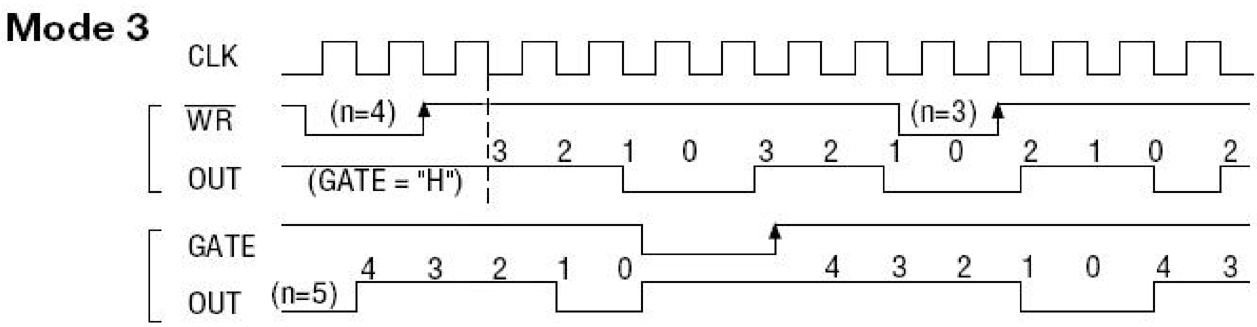


Figure 4

Mode 4: Software triggered strobe

Under this mode, the counter is given the initial count value N and begins to count, the output OUT becomes high level. When the count value becomes 0, it immediately outputs a negative pulse which is equal to the width of one clock cycle. If given a new count value when counting, it will be effective immediately. GATE=1 enables counting; GATE=0 disables counting. GATE has no effect on OUT. Time diagram is shown in figure 5.

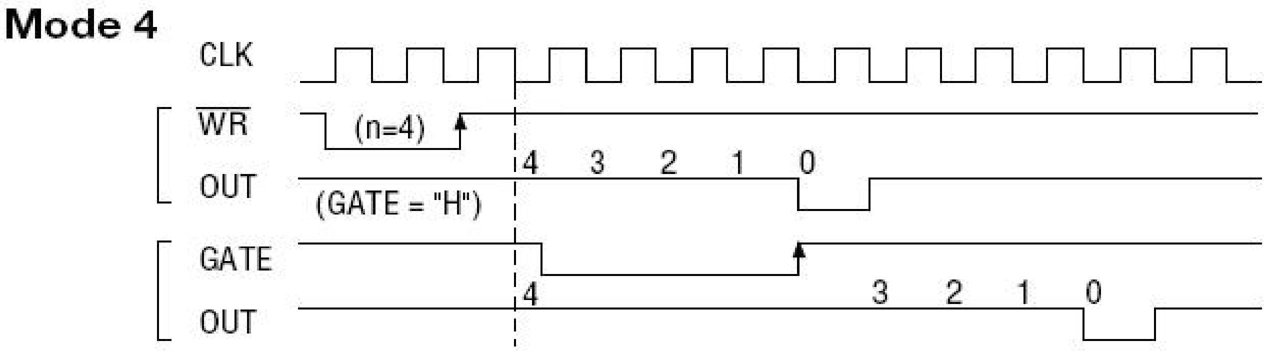


Figure 5

Mode 5: Hardware triggered strobe

Under this mode, when the signal of GATE is on the rising edge, the counter starts to count (so it is called hardware trigger), the output OUT has remained high level. When the count value becomes 0, it outputs a negative pulse which is equal to the width of one clock cycle. And then the rising edge of GATE signal can re-trigger, the counter starts to count from the initial count value again, in the count period, the output has remained high level. When the count reduction of the counter has not yet reached zero, but it is given a new value N1. Only when it is the rising edge of GATE, the counter starts to count from N1. Time diagram is shown in figure 6.

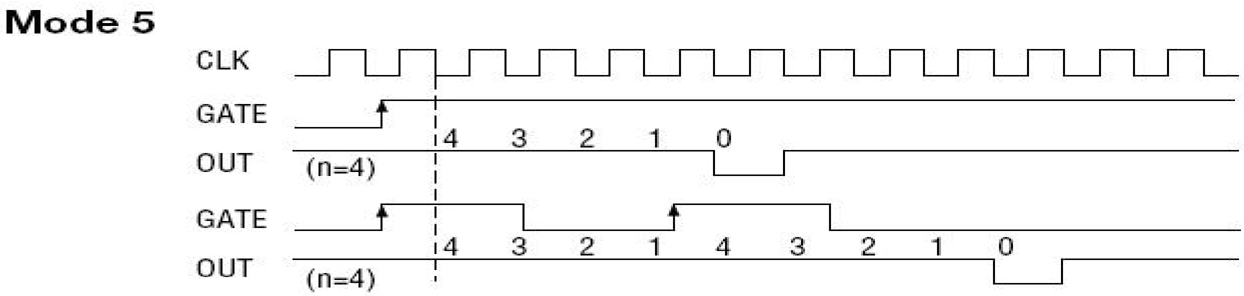


Figure 6

Chapter8 Notes, Calibration and Warranty Policy

8.1 Notes

In our products' packing, user can find a user manual, a PCI8305 module and a quality guarantee card. Users must keep quality guarantee card carefully, if the products have some problems and need repairing, please send products together with quality guarantee card to ART, we will provide good after-sale service and solve the problem as quickly as we can.

When using PCI8305, in order to prevent the IC (chip) from electrostatic harm, please do not touch IC (chip) in the front panel of PCI8305 module.

8.2 Analog Signal Input Calibration

Every device has to be calibrated before sending from the factory. It is necessary to calibrate the module again if users want to after using for a period of time or changing the input range. PCI8305 default input range: ±10V, in the manual, we introduce how to calibrate PCI8305 in ±10V, calibrations of other input ranges are similar.

Prepare a digital voltage instrument which the resolution is more than 5.5 bit, install the PCI8305 module, and then power on, warm-up for fifteen minutes.

1) Zero adjustment: Select AI0 for example; connect a DC voltage source with value equal to 0V to AI0.Adjust RP1 until the actual input value 0.000V.
2) Full-scale adjustment: Select AI0 for example; connect a DC voltage source with value equal to 9997.55mV to AI0. Adjust RP2 until the actual input value 9997.55mV.
3) Repeat steps above until meet the requirement.

8.3 Analog Signal Output Calibration

In the manual, we introduce how to calibrate PCI8305 in ±10V input range; calibrations of other input ranges are similar.

1) Zero adjustment: Select AO0 for example; set its output value to 0V. Adjust RP4 until the actual output value 0.000V. RP7, RP3, RP8 correspond to AO1, AO2, AO3.
2) Full-scale adjustment: Select AO0 for example; set its output value to 9995.11mV. Adjust RP6 until the actual output value 9995.11mV. RP9, RP5, RP10 correspond to AO1, AO2, AO3.
3) Repeat steps above until meet the requirement.

8.4 DA use

In demonstration program, the continuous output interval of waveform output can not be carried out; the main objective is to test the strength of DA output.

8.5 Warranty Policy

Thank you for choosing ART. To understand your rights and enjoy all the after-sales services we offer, please read the following carefully.

1. Before using ART's products please read the user manual and follow the instructions exactly. When sending in damaged products for repair, please attach an RMA application form which can be downloaded from: www.art-control.com.

2. All ART products come with a limited two-year warranty:

- The warranty period starts on the day the product is shipped from ART's factory
- For products containing storage devices (hard drives, flash cards, etc.), please back up your data before sending them for repair. ART is not responsible for any loss of data.
- Please ensure the use of properly licensed software with our systems. ART does not condone the use of pirated software and will not service systems using such software. ART will not be held legally responsible for products shipped with unlicensed software installed by the user.

3. Our repair service is not covered by ART's guarantee in the following situations:

- Damage caused by not following instructions in the User's Manual.
- Damage caused by carelessness on the user's part during product transportation.
- Damage caused by unsuitable storage environments (i.e. high temperatures, high humidity, or volatile chemicals).
- Damage from improper repair by unauthorized ART technicians.
- Products with altered and/or damaged serial numbers are not entitled to our service.

4. Customers are responsible for shipping costs to transport damaged products to our company or sales office.

5. To ensure the speed and quality of product repair, please download an RMA application form from our company website.

Products Rapid Installation and Self-check

Rapid Installation

Product-driven procedure is the operating system adaptive installation mode. After inserting the disc, you can select the appropriate board type on the pop-up interface, click the button【driver installation】; or select CD-ROM drive in Resource Explorer, locate the product catalog and enter into the APP folder, and implement Setup.exe file. After the installation, pop-up CD-ROM, shut off your computer, insert the PCI card. If it is a USB product, it can be directly inserted into the device. When the system prompts that it finds a new hardware, you do not specify a drive path, the operating system can automatically look up it from the system directory, and then you can complete the installation.

Self-check

At this moment, there should be installation information of the installed device in the Device Manager (when the device does not work, you can check this item.). Open "Start -> Programs -> ART Demonstration Monitoring and Control System -> Corresponding Board -> Advanced Testing Presentation System", the program is a standard testing procedure. Based on the specification of Pin definition, connect the signal acquisition data and test whether AD is normal or not. Connect the input pins to the corresponding output pins and use the testing procedure to test whether the switch is normal or not.

Delete Wrong Installation

When you select the wrong drive, or viruses lead to driver error, you can carry out the following operations: In Resource Explorer, open CD-ROM drive, run Others-> SUPPORT-> PCI.bat procedures, and delete the hardware information that relevant to our boards, and then carry out the process of section I all over again, we can complete the new installation.